ABSTRACT OF THE DISCLOSURE

Disclosed are a semiconductor memory device and a layout method thereof. The device comprises km memory cell array blocks arranged in the form of ak×m matrix, divided by x block selecting signals and y block selecting signals, and including a plurality of divided word lines arranged horizontally; a plurality of bit lines for each of the km memory cell array blocks arranged vertically; a plurality of main word lines for a plurality of bit lines for each of the km memory cell array blocks arranged horizontally; km of xy address word lines above or below the km memory cell array blocks; a decoder for decoding a corresponding x block selecting signal among x block selecting signals generated by decoding the x block selecting address and y block selecting signals generated by decoding the y block address to select corresponding m of xy address word lines and for being arranged for each of m memory cell array blocks arranged horizontally among the km memory cell array blocks; km of divided y address lines arranged vertically from the km of xy address word lines to the km memory cell array blocks; and word line driver for combining the plurality of the main word lines of each of the km memory cell array blocks and a signal of a corresponding xy address word line among the km of xy address word lines to select the plurality of the divided word lines and for being arranged for each of the km memory cell array block.

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